IN THE CLAIMS

1. (currently amended) An apparatus for packaging and providing backside access to an integrated circuit, the apparatus comprising:

a carrier substrate;

an array of package connection pads positioned around a periphery of a top surface of the carrier substrate;

a ring of die connection pads positioned within the array of package connection pads, the ring of die connection pads configured to provide electrical~~ly~~ connectivity to an integrated circuit die; and

an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die by removal of as much as all of the access region without damaging electrical integrity of any circuit traces of the carrier substrate.

2. (currently amended) The apparatus of claim ~~1~~ 3, wherein the carrier substrate comprises a plurality of circuit traces configured to electrically connect the array of package connection pads to the ring of die connection pads without penetrating the access region.

3. (currently amended) An apparatus for packaging and providing backside access to an integrated circuit, the apparatus comprising:

a carrier substrate;

an array of package connection pads positioned around a periphery of a top surface of the carrier substrate~~The apparatus of claim 1~~, wherein the array of package connection pads has a perimeter depth substantially equal to a maximum number of signal traces routable between minimally spaced package connection pads

a ring of die connection pads positioned within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die; and

an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die by removal of as much as all of the access region without damaging electrical integrity of any circuit traces of the carrier substrate.

4. (currently amended) An apparatus for packaging and providing backside access to an integrated circuit, the apparatus comprising:

a carrier substrate;

an array of package connection pads positioned around a periphery of a top surface of the carrier substrate~~The apparatus of claim 1~~, wherein the array of package connection pads has a perimeter depth that is less than a package connection pad spacing divided by a trace pitch

a ring of die connection pads positioned within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die; and

an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die by removal of as much as all of the access region without damaging electrical integrity of any circuit traces of the carrier substrate.

5. (currently amended) The apparatus of claim 3~~1~~, wherein the carrier substrate comprises a single signal layer.

6. (currently amended) The apparatus of claim 3~~1~~, wherein the access region corresponds to a substrate cavity.

7. (original) The apparatus of claim 6, wherein the integrated circuit die is positioned within the substrate cavity.

8. (original) The apparatus of claim 7, further comprising a package body molded over the integrated circuit die.

9. (currently amended) The apparatus of claim 3~~1~~, further comprising a heat spreader thermally connected to a bottom surface of the substrate.

10. (currently amended) The apparatus of claim 3~~-1~~, wherein the ring of die connection pads comprises a quadrant of bonding fingers that arc substantially equally distanced from an edge of the integrated circuit die.

11. (currently amended) The apparatus of claim 3~~-1~~, further comprising at least one grounding ring surrounding the access region.

12. (currently amended) The apparatus of claim 3~~-1~~, further comprising an array of solder balls attached to the array of package connection pads.

13. (currently amended) The apparatus of claim 3~~-1~~, wherein the carrier substrate is a printed circuit board.

14. (currently amended) The apparatus of claim 3~~-1~~, wherein the array of package connection pads is configured to receive an array of solder balls.

15. (previously presented) A method for designing an integrated circuit carrier with backside access to an integrated circuit, the method comprising:

placing an array of package connection pads around a periphery of a top surface of a carrier substrate;

placing a ring of die connection pads within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die; and

reserving an access region for conducting backside access to the integrated circuit die, wherein no signal traces are disposed.

16. (currently amended) The method of claim 17~~-15~~, further comprising placing at least one grounding ring surrounding the access region.

17. (currently amended) A method for designing an integrated circuit carrier with backside access to an integrated circuit, the method comprising:

placing an array of package connection pads around a periphery of a top surface of a carrier substrate.

placing a ring of die connection pads within the array of package connection pads, the ring of die connection pads configured to provide electrically connectivity to an integrated circuit die,

reserving an access region for conducting backside access to the integrated circuit die, wherein no signal traces are disposed, and

~~The method of claim 15, further comprising~~ selecting a perimeter depth for the array of package connection pads that is less than an package connection pad spacing divided by a trace pitch.

18. (currently amended) The method of claim 17 ~~15~~, further comprising selecting a quadrant shape for a quadrant of bonding fingers such that the bonding fingers are substantially equally distanced to an edge of an integrated circuit die.

19. (currently amended) The method of claim 17 ~~15~~, further comprising routing a plurality of traces between a ring of die connection pads and an array of package connection pads without penetrating the access region.

20. (previously presented) A method for packaging and providing backside access to an integrated circuit, the method comprising:

electrically connecting an integrated circuit die to a ring of die connection pads on a top surface of a carrier substrate;

attaching a cover to a bottom surface of the carrier substrate; and

removing a portion of the cover within an access region in order to access a backside of the integrated circuit without damaging any electrical connectivity of the substrate.

21. (original) The method of claim 20, further comprising placing the integrated circuit die within a cavity of the carrier substrate.

22. (original) The method of claim 20, further comprising molding a package body over the integrated circuit die.

23. (original) The method of claim 20, further comprising attaching an array of solder balls to the array of package connection pads.

24. (currently amended) A system for packaging and providing backside access to a wide variety of integrated circuits, the system comprising:

a plurality of circuit carriers, each circuit carrier configured to receive a range of integrated circuit sizes and ~~I/O~~ I/O counts, each circuit carrier overlapping in size range with at least one other circuit carrier of the plurality of circuit carriers, each circuit carrier comprising:

a carrier substrate;

an array of package connection pads positioned around a periphery of a top surface of the carrier substrate;

a ring of die connection pads positioned within the array of package connection pads; and

an access region positioned within the ring of die connection pads, the access region configured to facilitate backside access to the integrated circuit die by removal of as much as all of the access region without damaging electrical integrity of any circuit traces of the carrier substrate.

25. (original) The system of claim 24, wherein each circuit carrier overlaps in size range with no more than two other circuit carriers of the plurality of circuit carriers.